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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,747	06/27/2003	Dinh Bui	53597.1501	7706

7590 04/02/2004

AKIN, GUMP, STRAUSS, HAUER AND FELD
Attn: Mr. Clark A. Jablon
One Commerce Square
2005 Market Street, Suite 2200
Philadelphia, PA 19103

EXAMINER	
NGUYEN, LINH M	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 04/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/608,747	BUI ET AL.	
	Examiner	Art Unit	
	Linh M. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-21* is/are rejected.

7)☒ Claim(s) *5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *06/27/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-21 are presented in the instant application according to the Applicants' filing on 06/27/2003.

Inventorship

1. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-4 and 15-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Klein et al. (U.S. Patent No. 4,694,257).

With respect to claim 1, Klein et al. discloses, in Figure 2, a circuit having an external resistor [20] for establishing a delay of a signal [RX] relative to another signal [output(s) from 18] of the circuit.

With respect to claim 2, Klein et al. discloses, in Figure 2, a semiconductor device comprising a) an integrated circuit buffer [12, 20, 22, 14, 16, 18] that receives an input signal [RX] and generates a plurality of output signals [outputs from 18] that relate to the input signal, wherein the buffer includes a delay generator [12, 20, 22, 14, 16]; and a resistor [20] having a first resistor end that is electrically connected to the delay generator and a second resistor end that is electrically connected to ground or a voltage reference [Vcc], wherein the resistor is external to the integrated circuit buffer.

With respect to claim 3, Klein et al. discloses, in Figure 2, that the buffer comprises a zero-delay buffer.

With respect to claim 4, Klein et al. discloses, in Figure 2, the device is implemented on a circuit board and the external resistor is connected to a pin on a device package.

With respect to claim 15, Klein et al. discloses, in Figure 2, a circuit and its corresponding method of adjusting the timing of an output signal of a semiconductor device comprising the steps of a) electrically connecting a first terminal of an external resistor [20] to a buffer that generates a plurality of output signals [outputs from 18]; and b) electrically connecting a second terminal of the external resistor to a ground or a voltage reference [Vcc], wherein the buffer includes a delay generator [12, 20, 22, 14, 16]; and a phase locked loop [18], and the first terminal of the external resistor is electrically connected to the delay generator to adjust the timing of one or more of the output signals in an amount that is dependent upon the value of the external resistor.

With respect to claim 16, Klein et al. discloses, in Figure 2, that the buffer comprises a zero-delay buffer.

With respect to claim 17, Klein et al. discloses, in Figure 2, a semiconductor device, comprising a) an input terminal for receiving an input signal [RX], b) a buffer [12, 20, 22, 14, 16, 18]; for generating a plurality of output signals; and c) an external resistor [20] for altering a timing of one or more of the plurality of output signals relative to a timing of the input signal.

With respect to claim 18, Klein et al. discloses, in Figure 2, that the buffer comprises a zero-delay buffer.

With respect to claim 19, Klein et al. discloses, in Figure 2, that the device is implemented on a circuit board and the external resistor is connected to a pin on a package of the device.

With respect to claim 20, Klein et al. discloses, in Figure 2, that the adjusted output signals are phase-shifted to have a timing that is advanced or retarded relative to the input signal and the remaining output signals.

With respect to claim 21, Klein et al. discloses, in Figure 2, that a magnitude of the phase-shift is dependent upon a value of the external resistor.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 6-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Klein et al. (U.S. Patent No. 4,694,257) in view of Andresen et al. (U.S. Patent No. 5,355,037).

With respect to claims 6, 9, and 12, Klein et al. discloses all of the claimed limitations as expressly recited in claim 1, except for a) the phase locked loop includes a phase detector; and b) the delay generator, a delay line and the external resistor are electrically connected to adjust the timing of an internal feedback signal before the feedback signal reaches the phase detector.

Andresen et al. discloses, in Fig. 1, a phase locked loop with details including a) a phase detector, b) delay line and c) an internal feedback signal.

To configure the circuit of Klein et al. with a phase locked loop including details as taught by Andresen et al. having a phase detector, a delay line and an internal feedback to achieve high performance would have been obvious to one of ordinary skill in the art at the time of the invention since Andresen teaches that such configuration would facilitate high frequency clock synchronization *(see Andresen et al., col. 1, lines 6-9)*.

With respect to claims 7, 10 and 13, the combined teachings of Klein et al. (Fig. 2) and Andresen et al. (Fig. 2), disclose that the plurality of output signals are phase-shifted to have a timing that is advanced relative to the input signal.

With respect to claims 8, 11 and 14, the combined teachings of Klein et al. (Fig. 2) and Andresen et al. (Fig. 2), disclose that a magnitude of the phase-shift is dependent upon the value of the external resistor.

Allowable Subject Matter

6. Claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter:

The closest prior art on record does not show or fairly suggest: the device including a plurality of internal capacitors which are used in conjunction with an external resistor for providing a timing reference, each capacitor having a first capacitor end that is electrically connected to a current source and a second capacitor end that is electrically connected to ground or a voltage reference, as called for in claim 5.

Citation of Relevant Prior Art

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Prior art Cooper et al. (U.S. Patent No. 4,949,029) discloses an adjustment circuit and method for solid-state electricity meter with resistors connected externally to compensate the meter for phase.

Prior art Suh (U.S. Patent No. 5,754,071) discloses a delay circuit with an external resistor.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Linh M. Nguyen
Examiner
Art Unit 2816

LMN